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ECEN 5730
2/15/26
Board 2 Report

Project Overview:

Purpose: The purpose of this board is to gain practice with using good and bad layout practices and comparing outputs between 2 hex inverter circuits. Bad layout practices should result in higher switching noise.

POR:

1. Convert 5 V in to 3.3 V ; you learned this in lab #7.
2. Create a clock signal of about 500 Hz and about 50% duty cycle.
3. The hex inverters that we provide can operate at a 5 V or 3.3 V rail. Grad students must add a switch to control the hex inverter chips with either 5 or 3.3 V. This is optional for undergrads.
4. Add a switch to selectively connect the 555 output to either the good or bad layout hex inverters.
    a. When not connected to the timer output, all the switching inputs should be tied HIGH so they do not float and switch unpredictably. How will you implement this? (Hint, you learned this in lab #8).
5. Each hex inverter has six inputs. Drive four of the inputs to demonstrate good layout and bad layout.
6. On three of four outputs of each hex inverter use LEDs and 50 ohm resistors as the load. Connect the output of the fourth inverter to a test point to act as a trigger for the scope.
7. Estimate the current you expect to draw from the inverter for the LED and the 50 ohm resistor load.
8. Plan to extract the Thevenin resistance of the output pin of one of the I/O. (Hint: measure the voltage on the output of an inverter with the LED and resistor compared to the inverter with no load using a 10x probe and the scope. From the voltage drop on the I/O and the current draw, you can calculate the Thevenin resistance of the I/O pin.)
9. Of the two remaining inputs, set up one hex inverter as a quiet HIGH and inverter as a quiet LOW.
10. Use good debug techniques and add indicator LEDs, test points and circuit isolation switches as appropriate.
11. Engineer the layout on one side of the board with best design practices and the other side of the board with bad layout practices. In the bad layout, move the decoupling capacitors far away from the Vcc pin.

12. Keep the part placement and routing identical for the two regions of the board, except for the location of the decoupling capacitor.
13. A summary of test points for your board (I count 11):
    a. The scope trigger output
    b. The 555 output signal
    c. The 3.3. V rail on the board
    d. The 5 V rail on the board
    e. On both the good and bad
    f. Voltage across one of the 50 ohm resistors on both the good and bad
    g. The quiet high
    h. The quiet low
    i. The fourth inverter for a trigger and for the Thevenin Voltage measurement
14. Use best scope measurement practices when you test your board by using the 10X test points.
15. A power tree is a way to convey how each block of your circuit is powered.

Schematics:

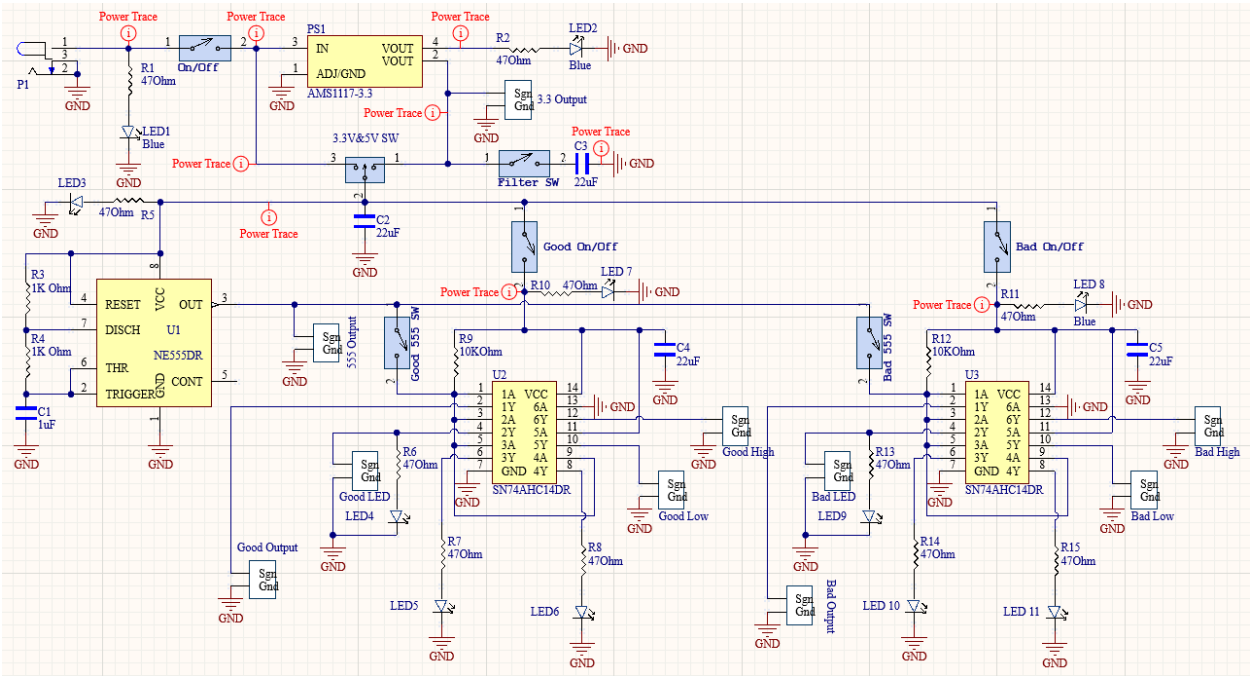


Figure 1: Schematic of the design in Altium Designer

Final Layout:

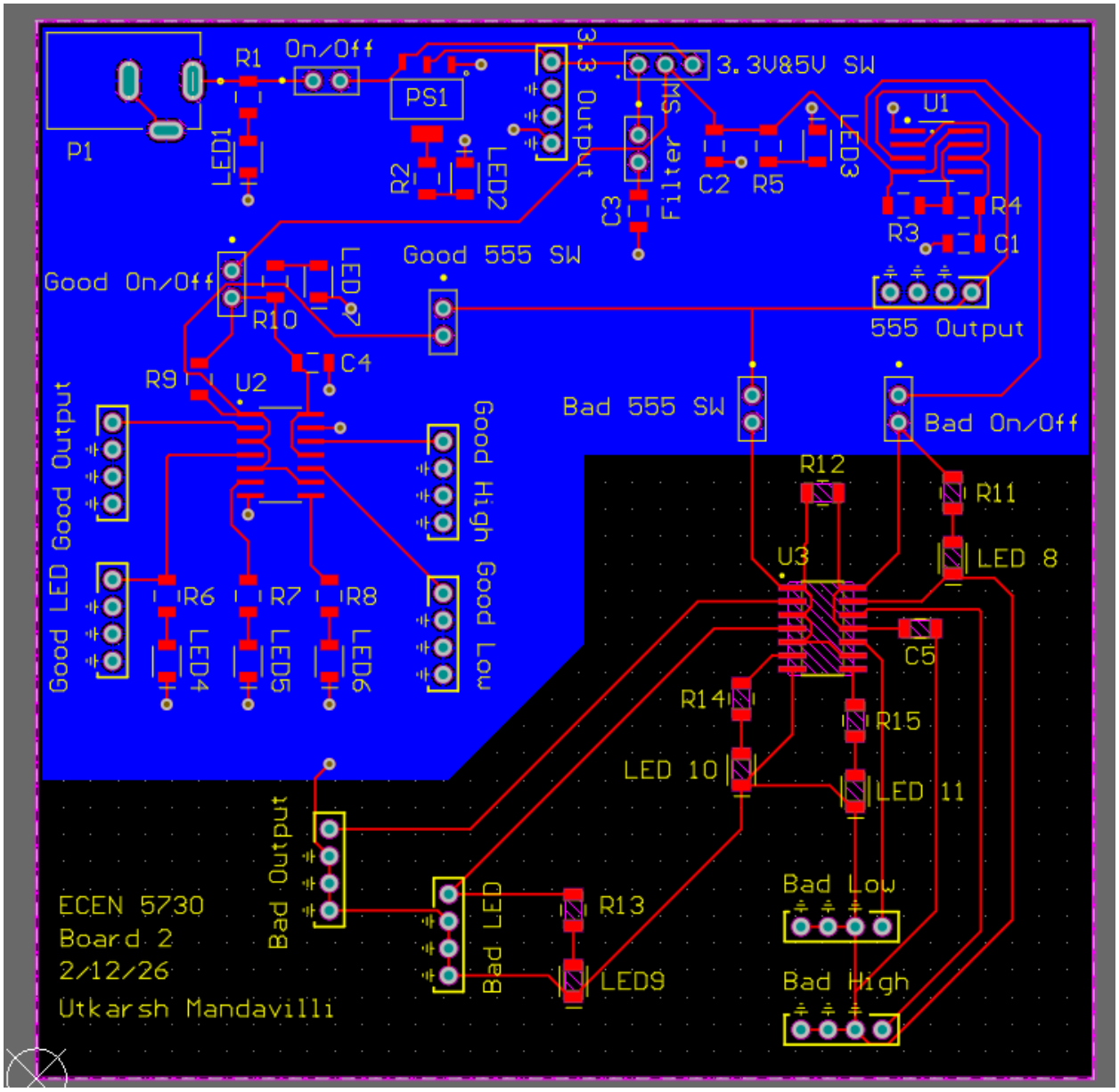


Figure 2: PCB Layout in Altium Designer

Pictures of the Board:

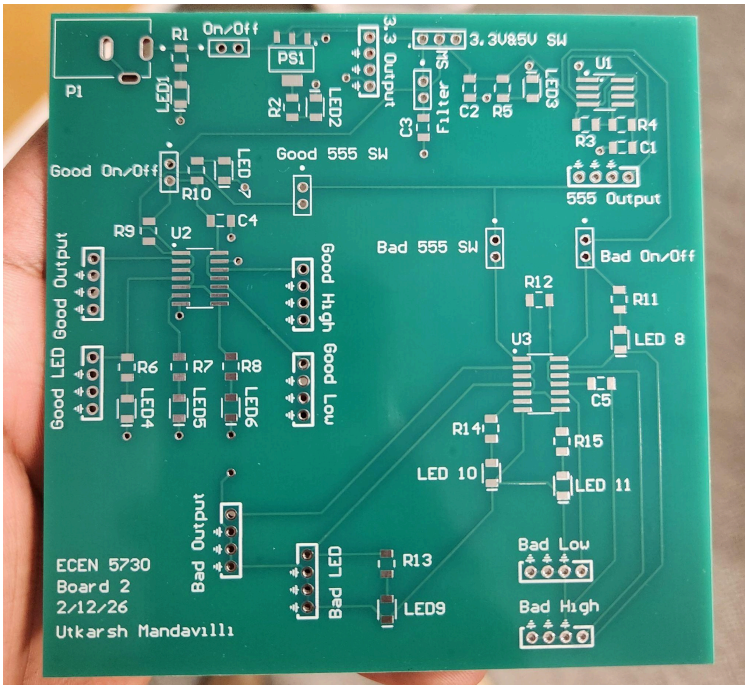


Figure 3: Picture of Unassembled Board

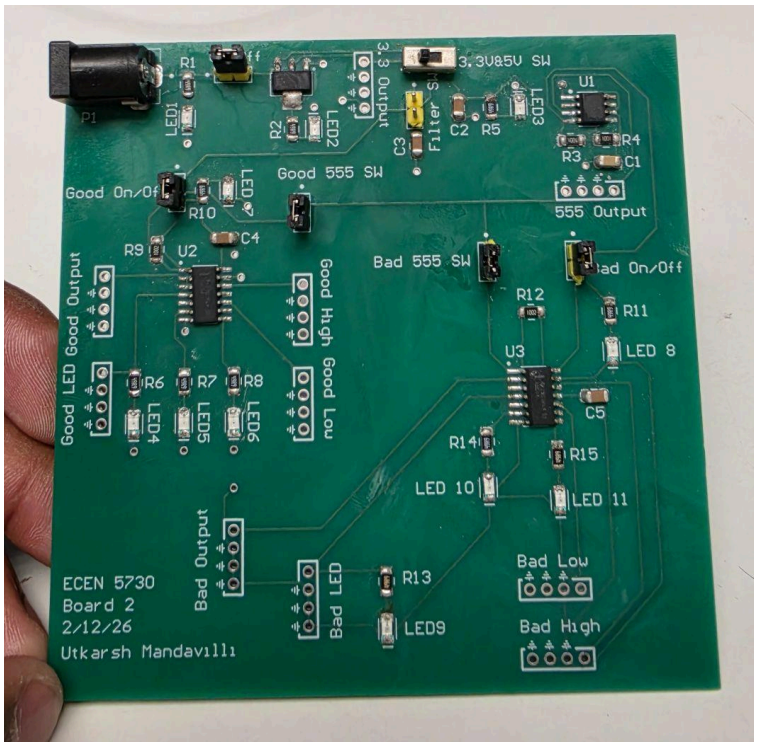


Figure 4: Picture of Assembled Board

Analysis of Board:

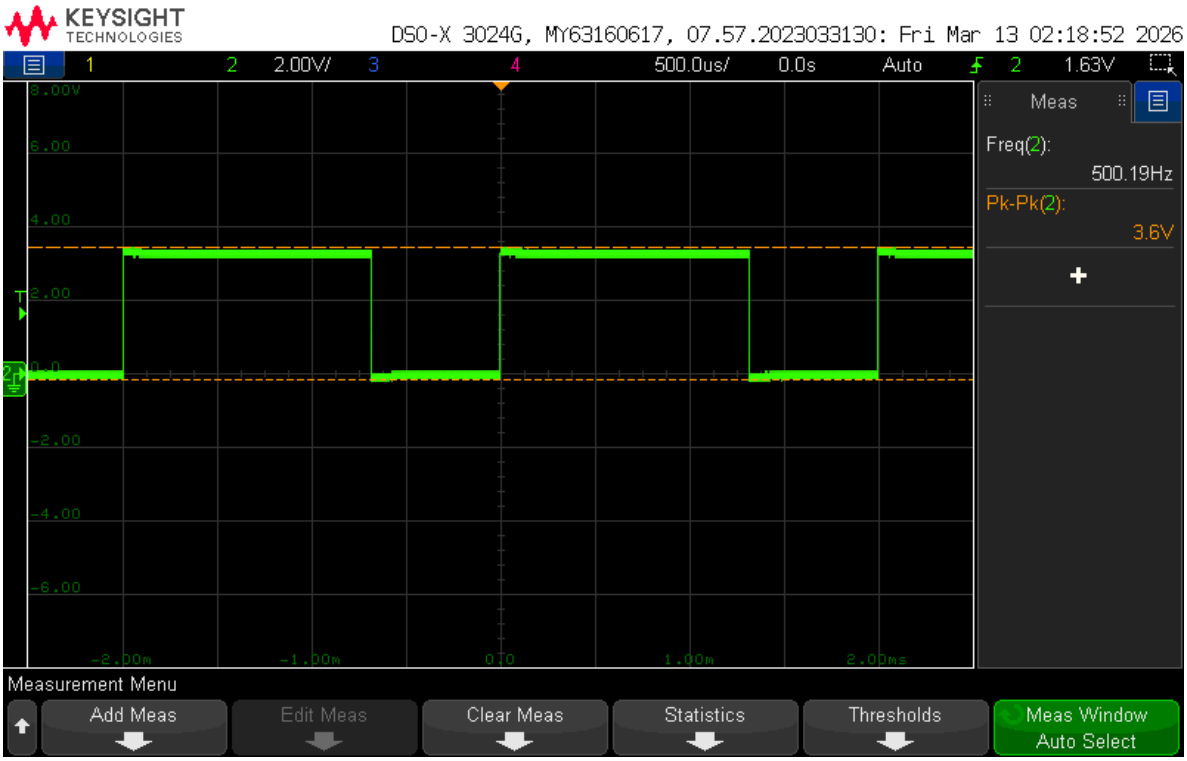
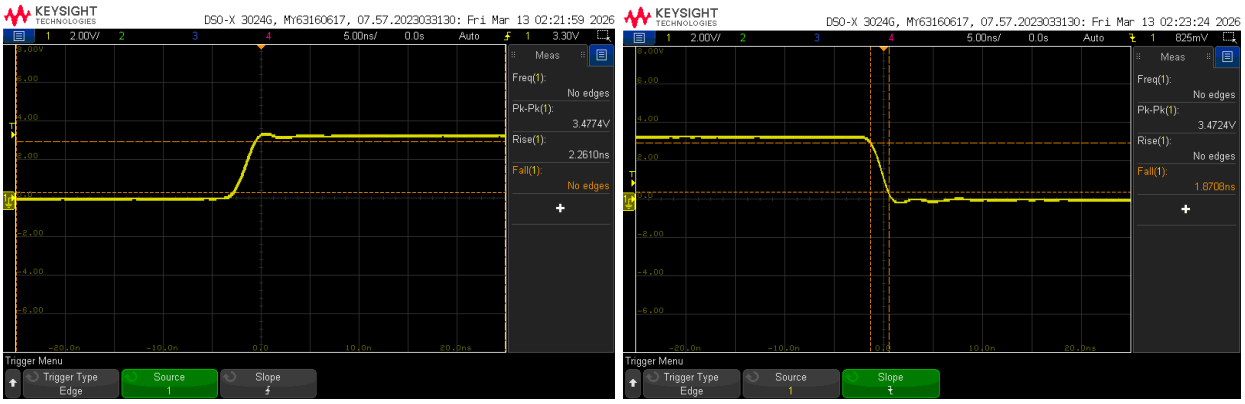


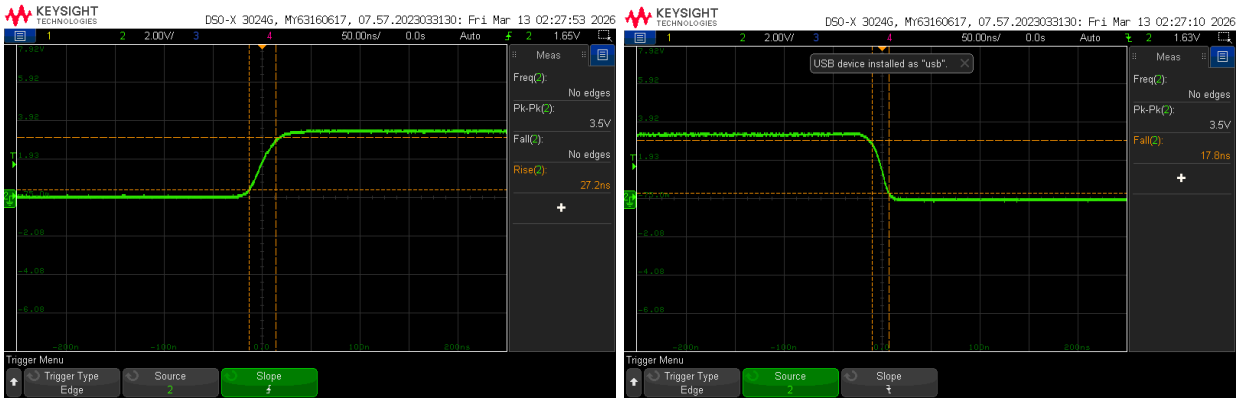
Figure 5: Output of the 555 timer.

The frequency and peak to peak voltage values are as expected. This circuit has an approximate duty cycle of 66%. This output is due to using the 3.3V power rail.



Figures 6&7: Rise and fall times of the 555 timer output. They are 2.35 and 1.87 ns, respectively.

These values are also expected when using the “fast” timer provided by the professor. Notice the output also has minimal noise and ground bounce.



Figures 8&9: Rise and fall times of the 555 timer output measured from the "Good" Hex Inverter. They are 27.3 and 17.8 ns respectively.

The slight difference in rise and fall times of the inverters is most likely due to the switching times of NMOS transistors as compared to PMOS transistors. They are able to pull the signal down at a quicker rate resulting in a faster falling edge. The signal is within the expected bounds and also shows minimal noise and ground bounce at the falling edge.

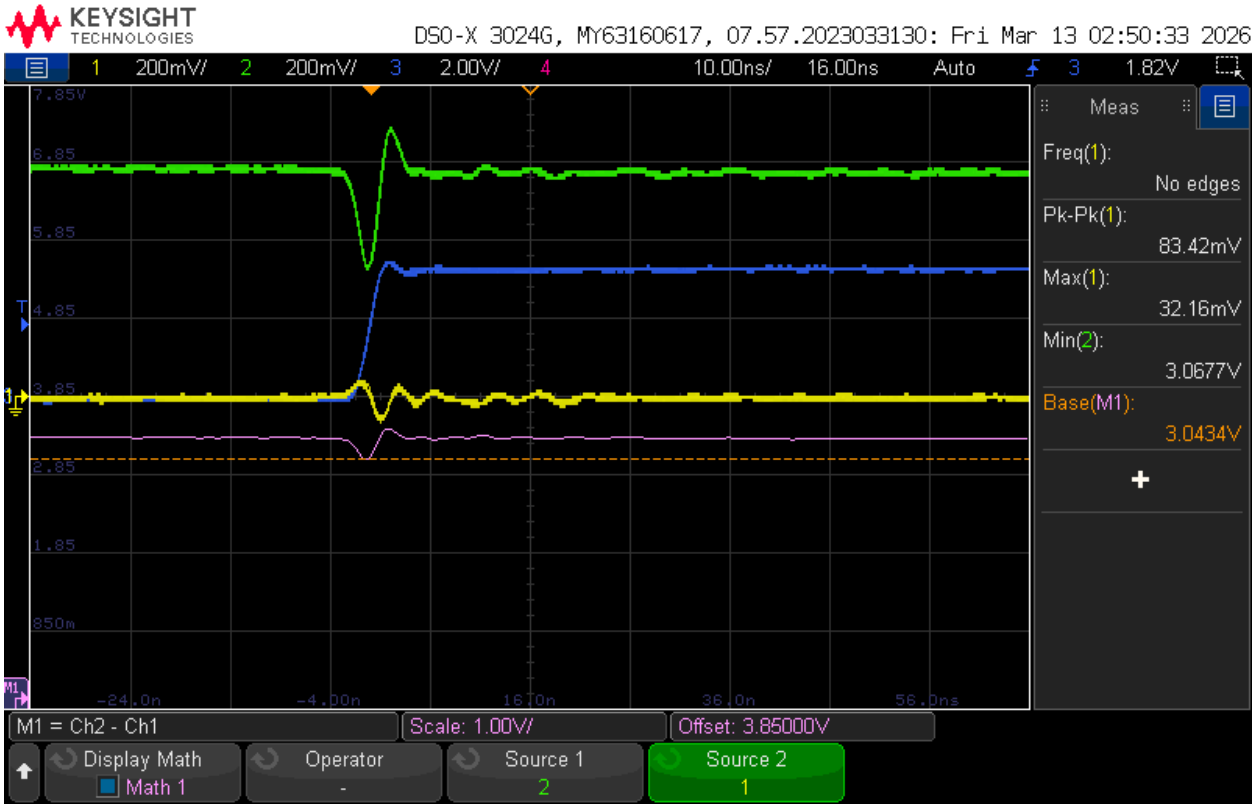


Figure 10: This scope measurement is of the "Good" Hex Inverter circuit. Green represents quiet high, Yellow represents quiet low, Blue represents the 555 timer output that triggers the scope, and Pink is the difference between quiet high and quiet low.

Here we see that once the 555 triggers we see a large voltage droop on the quiet high line. This indicates a large inrush current into the hex inverter circuit.

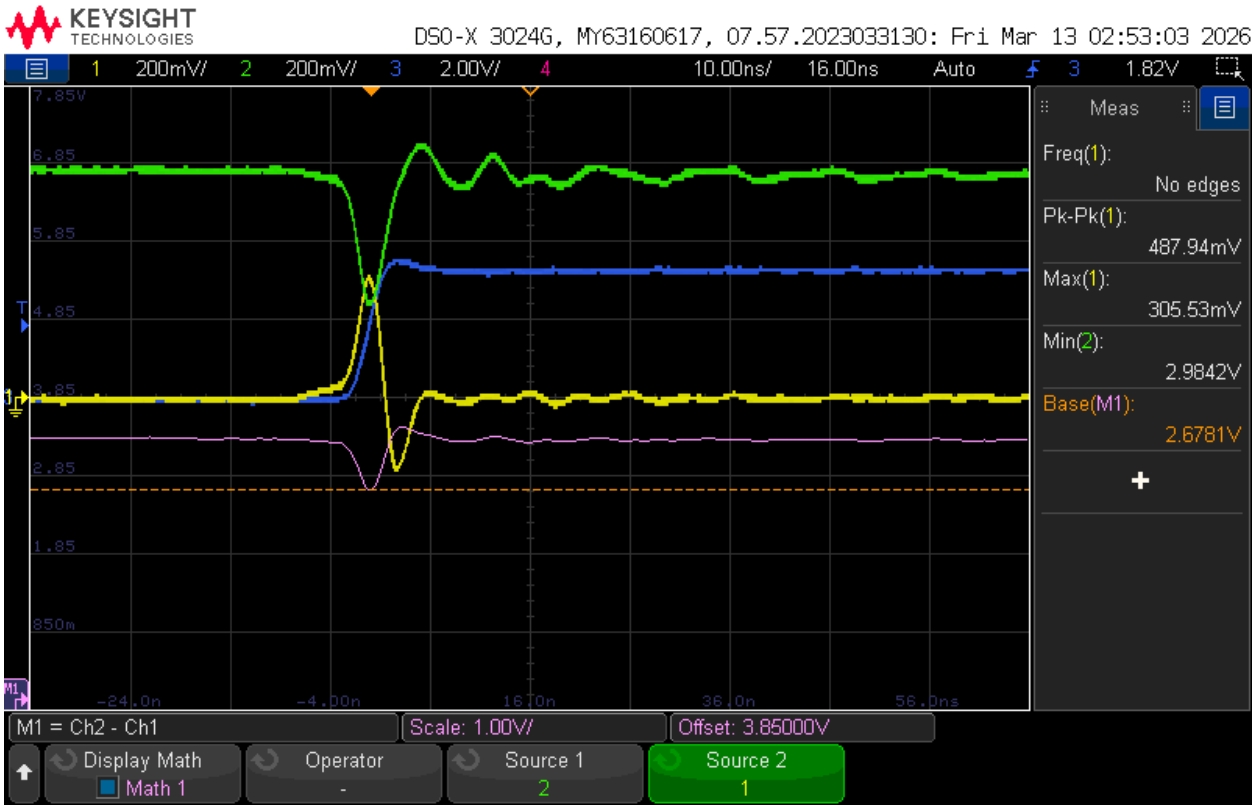
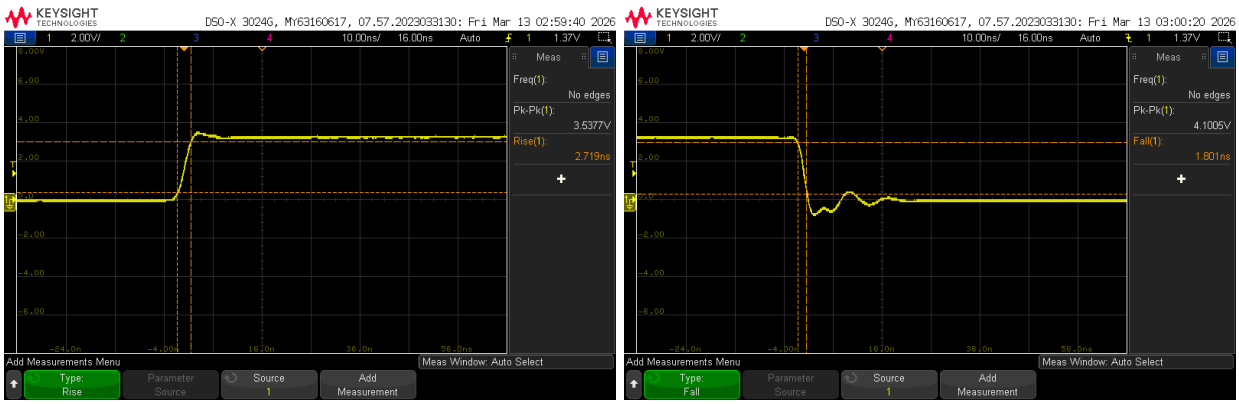


Figure 11: This scope measurement is of the "Bad" Hex Inverter circuit. Green represents quiet high, Yellow represents quiet low, Blue represents the 555 timer output that triggers the scope, and Pink is the difference between quiet high and quiet low.

These measurements are used to assess rail compression on each hex inverter circuit. This rail compression is a result of the quick switching speed and high voltages induced by the 555 timer output. The good circuit has far lower ground bounce than the bad circuit. The absence of a ground plane in addition to high inductances present in the circuit yields much higher spikes when switches in the input occur. The following equation models the change in voltage:

$$\Delta v = L\frac{di}{dt}$$

Both cases exhibit a similar voltage droop due to similar inductance paths in both circuits. Due to differences in ground bounce severity, the bad hex inverter circuit exhibits greater rail compression compared to the good one.



Figures 12&13: Rise and fall times of the 555 timer output from the bad hex inverter. They are 2.7 and 1.8 ns respectively.

These measurements are very close to the rise and fall times of the good hex inverter and are only 1-5ns longer. This difference in time is most likely due to longer traces and higher parasitic capacitances in the circuit. This is not what we expect to see and is most likely due to a short between the input and output of the hex inverter which causes identical times to the 555 timer.

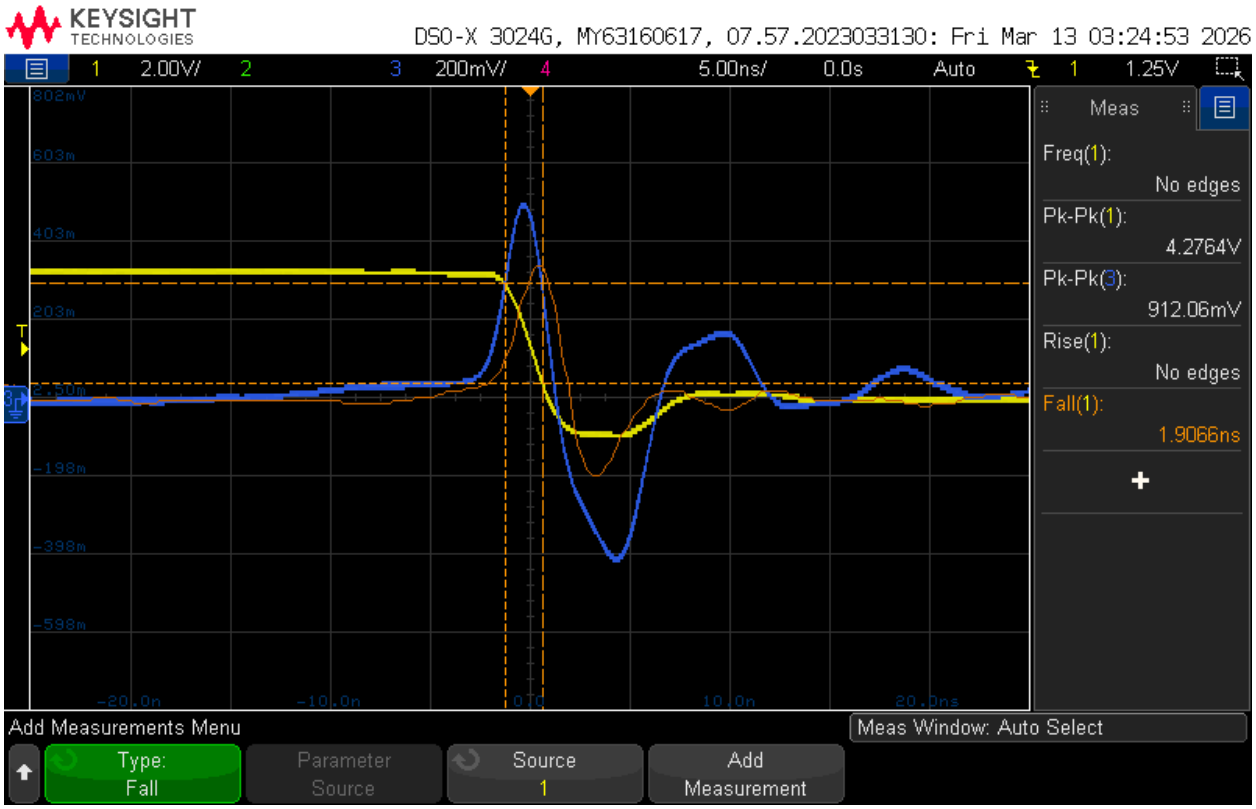


Figure 14: Scope measurement of the bad hex inverter. The Yellow is the falling edge of the hex inverter output, Blue is the quiet low without a 22 uF decoupling capacitor, and Orange is quiet low with a decoupling capacitor.

The presence of a decoupling capacitor reduces ground bounce to a great extent. When designing the circuit I forgot to place the capacitor near the power consuming elements, so moving the capacitor closer would yield even better results.

Conclusion:

Some key takeaways are the importance of a ground plane which can reduce ground bounce in signals. Decoupling capacitors can only do so much for ground bounce and a continuous ground plane becomes necessary. We also see how quick rise and fall times and higher voltage loads result in more pronounced voltage droop and ground bounce which is something that we can consider in future designs.